Soumya Ranjan Bhuyan

+91 891-745-3496 | soumyabhuyan687@gmail.com | LinkedIn | GitHub

SUMMARY

Eager Electronics & Tele-Comm Diploma Graduate with Design Verification expertise (Chipedge Certified). Skilled in System Verilog, Verilog, UVM, I2C/SPI, and AXI/APB protocols, with a results-driven approach to verification projects

TECHNICAL SKILLS

Programming Languages: C, Python,Shell scripting, Verilog, System Verilog, Oops
Other Skills: Logical Design, Linux, Windows, UVM, EDA, VCS, Xilinx, APB, AXI, I2C.
Soft Skills: Communication skills, Project management, Leadership, Public speaking, Teamwork.

PROJECTS

Verification of APB-Slave (DUT) using APB-Master (TB) Using SV Sep 2023 – Nov 2023
SV Testbench *System Verilog, APB, AXI*

- APB-Master's SV Testbench (V4.0) was implemented and connected to the APB-Slave DUT.
- DUT was tested with clock frequencies between 100MHz and 250MHz.
- Active low reset was used along with asynchronous assertion and desertion.
- APB is used to serve low-bandwidth peripherals and configure DUT registers.

Implemented APB-Master agent and whole Testbench using UVM Nov 2023 – Dec 2023
UVM Testbench *UVM, APB*

- APB-Master (V4.0)'s UVM-based Testbench was implemented.
- APB-Master Testbench and APB-Slave DUT related to clock frequencies between 100MHz and 250MHz.
- Used asynchronous assertion and desertion in conjunction with active low reset.

Implemented AXI-Master agent For Generic Incremental Burst using UVM Dec 2023 – Jan 2024
UVM, AXI

- Implemented the UVM based Testbench for AXI-Master (AXI3) and connected the AXI3-master Testbench to AXI-Slave DUT.
- The clock frequency at which The DUT is Tested is1Ghz.
- Real Application of AXI is Accessing Memory (RAM, FIFO and CACHE).
- AXI is a part of the AMBA protocol family interfaces to high bandwidth peripherals, and it is a pipelined protocol.

Personal Training

Design Verification Jul 2023 – Jan 2024
Chipedge Technologies Pvt. Ltd.

- Comprehensive Understanding of verification methodologies.
- Hands-on experience with HDLs.
- Effective testbench development.
- Simulation and debugging skills.

EDUCATION

C. V. Raman Global University Bhubaneswar
B. tech in Electronic & Tele-Communication Engineering *2020 – 2023*

Balasore School of Engineering Balasore
Diploma *2017 – 2020*

Public High School Balasore
Intermediate *2015 – 2017*