Md. Faizan Ahmad

Synthesis Engineer

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Career Objective

To secure a position in a reputable core electronics industry where I can leverage my technical, analytical, and professional skills to contribute to the organization's growth while allowing me to learn and implement new technology in VLSI by exploring it. I bring proven analytical abilities, a positive attitude, and adaptability to any circumstances to optimize the use of available resources.

Academic Qualification

B.Tech (Electronics and Communication Engineering) — *2020 - 2024*
- Bhagwan Parshuram Institute of Technology Guru Govind Singh Indraprastha University Delhi, India

Percentage- 85

Intermediate — *2019 - 2020*
- Kendriya Vidyalaya No. 3 Delhi Cantt 10

Percentage- 69

Matriculate — *2017 - 2018*
- Kendriya Vidyalaya No. 3 Delhi Cantt 10

Percentage- 76

Skills

- **Technical Skills** : Synthesis, Digital Logic Design, Physical Design, Static Timing Analysis (STA), Verilog HDL, System verilog, Analog Design, TCL, C/C++
- **Software** : Cadence Genus, Cadence Innovus, Cadence Cerebrus, Cadence Virtuoso, Jed AI, Xilinx ISE

Experience

★ **Synthesis R & D Intern** — **Sept 2024 - Sept 2025**

Cadence Design Systems, Hyderabad, India

- Gained hands-on experience with industry-standard EDA tools: Genus (synthesis), Innovus (physical design), LEC (logic equivalence checking), JedAI (data analytics), Cerebrus (ML-based optimization), and Chipware (IP Components)
- Explored advanced synthesis techniques, including PPA (Power, Performance, Area) trade-offs, multi-bit register optimization, retiming and clock gating techniques.
- Developed proficiency in Tcl scripting, applying it for tool automation, synthesis flow customization, and optimization strategies.
- Contributed to a customer-facing project integrating Genus and JedAI with an AI-powered Copilot chatbot, enabling real-time design queries and analysis by performing testing and validation, proposing feature and data improvements, and conducting chatbot assessments across multiple customer designs.
- Designed a Tcl-based framework for enabling AI agents to interface with Genus; integrated with Python and LLMs to support real-time, automated responses to design-related queries by dynamically invoking appropriate agents within Genus.

★ **Physical Design Trainee** **July 2023 - Sept 2024**
Pine Training Academy, Noida, India

- Gained hands-on experience in designing various digital hardware components such as Half Adder, Full Adder, Multiplier, Divider, Mux & Demux using Schematic design and implemented them on FPGA Board to verify and validate functionality.
- Worked on complete Physical Design flow on a design of 4 blocks, from floorplanning to routing, Performed static timing analysis (STA) to resolve timing violations, conducted various sanity checks to ensure design clearance and applied different techniques to fix the congestion issue in design.

Projects

Hardware Digital Design

Implementation of AES Algorithm for Enhanced Confidentiality in UART Serial Communication

- **Tool / Technology Used** : VHDL, UART, BASYS 3 FPGA, Tera Term, Xilinx Vivado 2020.2, AES
- **Description** : Designed a system for secure serial communication utilizing symmetric cryptography where AES is used to encrypt and decrypt a 128 bit plain text with a fixed key and output carried out by UART and displayed on tera term along with hardware simulation on BASYS 3 FPGA to verify the effectiveness of the algorithm.

Designing of 4 - Bit Sign Calculator

- **Tool / Technology Used** : Xilinx ISE, FPGA
- **Description** : Designed a 4 - Bit Sign calculator using different modules such as Adder/Subtractor, Multiplier/divider & Mux/Demux using A Schametic Design to perform a simple arethematic calculation of 4 Bit data and implemented on FPGA

Scripting

Log File Analyzer & Placement Sanity Checker

- **Tool / Technology Used** : Linux
- **Description** : A TCL Script was written to perform a differnt placement checks like reporting of macros status, floating terms, Don't-use cells, missing lefs, multidriven/undriven nets during the Placement stage in PNR along with writing out a log file which analyzed separately by the script for providing file info and finding out different types of errors and warnings encountered at different stages of PNR.

Certifications

- Certified trainee of Pine training Academy in Physical Design & Synthesis Domian
- Certificate of completion in Basics of Remote Sensing, Geographical Information System & Global Navigation Satellite System — IIRS-ISRO